AMENDMENTS

In the Specification

Please replace the paragraph on page 3, lines 20-30 with the following amended paragraph:

In some networks, network nodes store data that are used for proper operation. In SONET, data between adjacent nodes are transmitted in modules called STS's (synchronous transport signals). Each STS is transmitted on a link at regular time intervals (for example, 125 microseconds). See Bellcore Generic Requirements document GR-253-CORE (Issue 2, December 1995) incorporated herein by reference. An STS-1 ~~is a~~ (Synchronous Transport Signal-level 1) is the basic module in SONET and is defined as a specific sequence of 810 bytes (6480 bits), including overhead bytes and an envelope capacity for transporting payloads. In general, the higher-level signals, the STS-N signals, are lower-level modules that are multiplexed together and converted to an OC-N or STS-N signal. An STS-N frame is a sequence of N x 810 bytes wherein N is a predetermined number. An STS-N is formed by byte-interleaving of STS-1 and STS-M modules, wherein M is less than N.

Please replace the paragraph on page 6, lines 17-19 with the following amended paragraph:

Fig. 8 is a circuit diagram of elements of a pointer processor that operate to cause an AIS ~~sugnal~~ **signal** to be generated at the output of all processors when an ~~errir~~ **error** is detected at any one of the processors.

Please replace the paragraph beginning on page 9, line 22 and ending on page 10, line 2 with the following amended paragraph:

Using signal paths 200 as an example, data enters the system at one of line cards 220(1,1)-(N,N). It is at this point, in a SONET-based system, that the Section and Line overheads are processed and stripped off by a protocol processor (not shown). The extracted SONET/SDH payload envelope is then synchronized with the system clock and sent to two different copies of a local matrix, depicted as group matrices 212(1)-(N) and 216(1)-(N) in ~~Fig. 1A~~ **Fig. 2**. In one embodiment, group matrices 212(1)-(N) and 216(1)-

(N) are used mainly as 2:1 reduction stages that select one of two optical signals and pass the selected optical signal to switching matrix 130. This allows the implementation of a variety of protection schemes (including 1:N, or 0:1) without having to use any additional ports on main matrix 214. All protect signals are terminated at group matrices 212(1)-(N) and 216(1)-(N). In order to maximize bandwidth, it is preferable that only active signals be passed through to switching matrix 130.

Please replace the paragraph on page 14, lines 14-18 with the following amended paragraph:

In order to add protection channels, line-side optical transmitter ~~410~~ **411** is also coupled to a 1:2 broadcast unit 435. To receive such optical signals, optical receiver 406 is also coupled to a 2:1 selector 436 in order to select the working channel before the optical signals leave the shelf and thus prevent the standby channel (also referred to herein as the protect channel) from using any bandwidth on switching matrix 130.

Please replace the paragraph on page 17, lines 10-16 with the following amended paragraph:

Switching matrix 130 is based on a rearrangeably non-blocking switching matrix and can consist, for example, of switch nodes arranged in a staged array. For example, switching matrix 130 configured as a 256x256 switching matrix consists of 48 nodes arranged in an array of 16 rows by 3 columns, with each column containing one stage. All 48 nodes in the ~~switch~~ **switching** matrix are substantially similar. Each node is preferably a crossbar device, such as a 16x16 crossbar device that allows any of its 16 inputs to be connected to any of its 16 outputs, regardless of the crossbar's current state.

Please replace the paragraph on page 19, lines 11-21 with the following amended paragraph:

Referring now to Figure 8, the pointer processor generates an Error Detection signal that is assumed to be negative-going. The Error Detection signal may, in a preferred embodiment, be programmable and derived from SONET failure signals, such as, LOS (Loss of Signal), LOF (Loss of Frame), OOF (Out of Frame), AIS_L or LOP_P, or may result when a processor detects that an STS_Nc is not present. In any event, the

occurrence of an Error Detection signal is coupled through an inverter 81 to input of a ~~Wire-Or'd~~ **Wired-OR** transistor Q1. When transistor Q1 becomes conductive, a logic ZERO will be asserted at the bidirectional pin of the detecting processor. The logic ZERO will also appear at the bidirectional terminal, 72Xc, of the other processors. Either the Error Detection signal or the logical ZERO at the bidirectional terminal will cause an alarm signal, AIS, to appear at each of the processor outputs 721b, 722b, 723b, and 724b.